

Abstract

**CLOCK DISTORTION DETECTOR USING A SYNCHRONOUS
MIRROR DELAY CIRCUIT**

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The invention refers to a clock distortion detection method, and a clock distortion detector including a first input for receiving a first clock signal, a second input for receiving a second clock signal, and at least one
10 mirror delay element.

Reference Numbers

1a synchronous mirror delay element
1b synchronous mirror delay element
5 1c synchronous mirror delay element
1d synchronous mirror delay element
2 MOSFET
3 MOSFET
4 MOSFET
10 5 MOSFET
6 MOSFET
7 MOSFET
8 MOSFET
9 MOSFET
15 10a line
10b line
10c line
10d line
10e line
20 10f line
10g line
10h line
10i line
10k line
25 10l line
10m line
10n line
10o line
10p line
30 11a line
11b line
12 clock distortion detector
14 clock line
15 clock line
35 16 test control device
17 mirror delay circuit